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PCI Express Retimer Test Specification

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1. Coverage

This test Specification is intended to confirm if a retimer is compliant to the PCIe 4.0 Base Specification.

It does not cover retimers based on the Retimer ECN to the PCIe 3.0 specification.

2. Electrical Tests

All 16 GT/s Electrical Tests defined in the PCI Express Base Specification Revision 4.0 Version 1.0 are required for re-timers. A replica channel which reproduces the electrical characteristics of the breakout channel as closely as possible, matching its length, layer transitions, etc, is required on the re-timer evaluation board for making it possible to de-embed Tx measurements to the pin of the DUT. Refer to the PCI Express Base Specification, (sections 8.3.1 and 8.4.1) for more details on the Electrical tests and replica channel guidelines.

2.1 Impedance Propagation Test (Informative)

This test determines if a retimer correctly propagates receiver impedance.

1. Place the DUT on a link between 2 exercisers with the Z_Rx of both set to a High Impedance (>20K ohms).
2. Follow the procedure described in Section 3.1 Retimer Reset Macro to reset the retimer.
3. Confirm that the neither Transmitter attempted to exit Electrical Idle. %could be done, but would take work on the exerciser side - may not be easily measurable
4. Set the Z_Rx of the downstream exerciser to a Low Impedance (between 40 and 60 ohms).
5. Confirm that the Z_Rx seen on the retimer by the upstream exerciser transitions to between 40 and 60 ohms within 1.0 ms.
6. Set the Z_Rx of the upstream exerciser to a Low Impedance (between 40 and 60 ohms).
7. Confirm that the Z_Rx seen on the retimer by the exerciser acting as a downstream port transitions to between 40 and 60 ohms within 1.0 ms.

3. Test Macros

3.1 Retimer Reset Macro

This macro performs a Fundamental Reset of the retimer.

- If the Retimer supports the CEM form factor:

1. Assert PERST# on the upstream pseudoport for 200 µS.
2. De-assert PERST# and wait 20 ms.

- Otherwise, perform a retimer- or form-factor-specific Reset.

3.2 Retimer Training Set Forwarding Macro

This macro puts the retimer into a state where it is forwarding training sets, as described in section 4.3.6.1 of the PCIe 4.0 Specification.

1. Follow the procedure described in Section 3.1 Retimer Reset Macro to reset the retimer.
2. Wait up to 30 ms for the retimer to determine receiver impedance on both sides
3. Wait up to 2 ms for the impedance to be back-propagated to the other side of the pseudo port.
4. Send 32 consecutive TS1s to the retimer with contents described in either Table 3-1 Retimer 8b/10b Training Set 1 Contents or Table 3-2 Retimer 128b/130b Training Set 1 Contents .

Table 3-1 Retimer 8b/10b Training Set 1 Contents

Offset		Description	Value
Symbol	Bit		
0	-	Symbol Alignment	K28.5
1	-	Link Number	0h
2	-	Lane Number within Link	Port Lane number
3	-	N_FTS - Number of Fast Training Sequences required by the Receiver	0
4	Data Rate Identifier		
	0	Reserved	0b
	1	2.5 GT/s Data Rate Supported	1b
	2	5.0 GT/s Data Rate Supported	1b
	3	8.0 GT/s Data Rate Supported	1b
	4	16.0 GT/s Data Rate Supported	1b
	5	Reserved	0b
	6	Autonomous Change or Selectable De-emphasis	Exerciser-Specific
	7	Speed Change	0b unless changing data rate
5	Training Control		
	0	Hot Reset	0b

Offset		Description	Value
Symbol	Bit		
	1	Disable Link	0b
	2	Loopback	0b
	3	Disable Scrambling	0b
	4	Compliance Receive	0b
	7:5	Reserved	000b
6	-	TS1 Identifier (or TS1 Equalization when applicable)	D10.2 (4Ah)
7 - 15	-	TS1 Identifier	D10.2 (4Ah)

Table 3-2 Retimer 128b/130b Training Set 1 Contents

Offset		Description	Value
Symbol	Bit		
0	-	TS1 Ordered Set Identifier	1Eh
1	-	Link Number	0h
2	-	Lane Number within Link	Port Lane number
3	-	N_FTS - Number of Fast Training Sequences required by the Receiver	0
4	Data Rate Identifier		
	0	Reserved	0b
	1	2.5 GT/s Data Rate Supported	1b
	2	5.0 GT/s Data Rate Supported	1b
	3	8.0 GT/s Data Rate Supported	1b
	4	16.0 GT/s Data Rate Supported	1b
	5	Reserved	0b
	6	Autonomous Change or Selectable De-emphasis	Exerciser-Specific
	7	Speed Change	0b unless changing data rate
5	Training Control		
	0	Hot Reset	0b
	1	Disable Link	0b
	2	Loopback	0b

Offset		Description	Value
Symbol	Bit		
	3	Reserved	0b
	4	Compliance Receive	0b
	7:5	Reserved	000b
6	1:0	EQ control	00b unless in Recovery.Equalization
	2	Reset EIEOS Interval Count	0b
	6:3	Transmitter Preset	0b unless in Recovery.Equalization
	7	Use Preset/EQ Redo	0b unless in Recovery.Equalization
7	5:0	FS/Pre-Cursor Coefficient	Exerciser-Specific
	6	Reserved	0b
	7	Retimer Eq Extend	0b unless in Recovery.Equalization
8	5:0	LF/Cursor Coefficient	Exerciser-Specific
	7:6	Reserved	00b
9	5:0	Post-cursor Coefficient	Exerciser-Specific
	6	Reject Coefficient Values	0b unless in Recovery.Equalization
	7	Parity	Dependant on Exerciser-Specific bit contents
10-13	-	TS1 Identifier	4Ah
14-15	-	TS1 Identifier or DC Balance	4Ah or DC Balance Symbol

3.3 Retimer Non-Training Set Forwarding Macro

This macro puts the retimer into a state where it is forwarding non-training sets, as described in section 4.3.6.1 of the PCIe 4.0 Specification.

1. Follow the procedure in Section 3.2 Retimer Training Set Forwarding Macro to get the retimer into a state where it is Forwarding Training Sets.
2. Send 32 TS2s to the retimer with contents described in either Table 3-3 Retimer 8b/10b Training Set 2 Contents or Table 3-4 Retimer 128b/130b Training Set 2 Contents .

3. Send 16 consecutive symbols of IDL on all lanes that are forwarding symbols (see section 4.2.2.3.1).

Table 3-3 Retimer 8b/10b Training Set 2 Contents

Offset: Symbol	Offset: Bit	Description	Value
0	-	Symbol Alignment	K28.5
1	-	Link Number	0h
2	-	Lane Number within Link	Port Lane number
3	-	N_FTS - Number of Fast Training Sequences required by the Receiver	0
4	Data Rate Identifier		
	0	Reserved	0b
	1	2.5 GT/s Data Rate Supported	1b
	2	5.0 GT/s Data Rate Supported	1b
	3	8.0 GT/s Data Rate Supported	1b
	4	16.0 GT/s Data Rate Supported	1b
	5	Reserved	0b
	6	Autonomous Change or Selectable De-emphasis	Exerciser-Specific
	7	Speed Change	0b unless changing data rate
5	Training Control		
	0	Hot Reset	0b
	1	Disable Link	0b
	2	Loopback	0b
	3	Disable Scrambling	0b
	4	Retimer Present in 2.5 GT/s data rate. Reserved in 5.0 GT/s data rate.	0b
	5	Two Retimers Present in 2.5 GT/s data rate. Reserved in 5.0 GT/s data rate.	0b
	7:6	Reserved	00b
6	-	TS2 Identifier (or TS2 Equalization when applicable)	D5.2 (45h) (Exerciser-Specific for TS2 Equalization OS)
7 - 15	-	TS2 Identifier	D5.2 (45h)

Table 3-4 Retimer 128b/130b Training Set 2 Contents

Offset		Description	Value
Symbol	Bit		
0	-	TS2 Ordered Set Identifier	2Dh
1	-	Link Number	0h
2	-	Lane Number within Link	Port Lane number
3	-	N_FTS - Number of Fast Training Sequences required by the Receiver	0
4	Data Rate Identifier		
4	0	Reserved	0b
4	1	2.5 GT/s Data Rate Supported	1b
4	2	5.0 GT/s Data Rate Supported	1b
4	3	8.0 GT/s Data Rate Supported	1b
4	4	16.0 GT/s Data Rate Supported	1b
4	5	Reserved	0b
4	6	Autonomous Change or Selectable De-emphasis or Link Upconfigure Capability	Exerciser-Specific
4	7	Speed Change	0b unless changing data rate
5	Training Control		
5	0	Hot Reset	0b
5	1	Disable Link	0b
5	2	Loopback	0b
5	7:3	Reserved	00000b
6	4:0	Reserved	00000b
6	7:5	Reserved	000b
7	-	TS2 Identifier	45h
8-13	-	TS2 Identifier	45h
14-15	-	TS2 Identifier or DC Balance	45h or DC Balance Symbol

3.4 Retimer Data Rate Change Macro

This macro is used to transition the retimer from one data rate to another

1. Enter Electrical Idle using the process described in Section 3.5 Electrical Idle Entry Macro at the current data rate.
2. Remain in Electrical Idle for 2 ms.
3. Exit Electrical Idle at the desired data rate using the process described in Section 3.6 Electrical Idle Exit Macro .

3.5 Electrical Idle Entry Macro

This macro is used to transition a retimer pseudoport into electrical idle.

1. Send an EIOSQ from both exercisers on all lanes.

3.6 Electrical Idle Exit Macro

This macro is used to transition a retimer out of electrical idle.

1. From one exerciser, send 2 (or more) consecutive TS1's at the desired data rate on all lanes with Lane and Link Number set to PAD.
2. Use the process described in Section 3.2 Retimer Training Set Forwarding Macro to forward training sets at the desired data rate.

3.7 Lane Margining Macro

This macro is used to place the link into and out of the lane margining State

1. If not already forwarding training sets, use the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro to begin forwarding training sets at 16GT/s.
2. To enter the lane margining state, transmit a "Report Margin Control Capabilities" Control SKP Ordered Set.
3. To exit the lane margining state, transmit a "Go to Normal Settings" Control SKP Ordered Set.

4. Logical Retimer Tests

4.1 Retimer Logical Test Setup

Most Logical retimer tests require the use of two PCIe Exercisers, One connected to the Retimer's Upstream Pseudoport and the other connected to the Retimer's Downstream Pseudoport. To ensure the retimer meets the specifications timing requirements, the Exercisers must be capable of recording when a packet arrives accurate to at least 5 nanoseconds.

Some tests require the use of an external clock source capable of supplying two separate reference clocks with a relative difference (ex: 200ppm) to the exercisers.

In order to conduct the Logical tests, Manufacturers must supply the Retimer attached to an Evaluation Board as described in Chapter 2 of the PCI Express Architecture Link Layer and Transaction Layer Test Specification, Revision 4.0. The CEM Connector and the Upstream Pseudoport must be connected to Add-in Card Edge. The Add-in Card Edge and CEM connector must be at least as wide as the maximum number of lanes supported by the retimer.

4.2 SKP OS Add/Remove Test

1. Place the DUT on a link between 2 exercisers.
2. Configure the upstream exerciser to operate with a clock that is 100 ppm faster than the downstream exerciser.
3. For every data rate supported by the DUT:
    1. Get the retimer into a state where it is forwarding data in both directions using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. for 8b/10b encodings:
        1. Have the exercisers insert a SKPOS between every 1185 symbols.
        2. Confirm that the retimer is adding 1 SKP symbol to at least 1 SKPOS per 1538 * 10^4 symbols in the upstream direction.
        3. Confirm that the retimer is removing 1 SKP symbol to at least 1 SKPOS per 1538 * 10^4 symbols in the downstream direction.
        4. Have the exerciser insert a SKPOS between every 1533 symbols and confirm the above SKPOS addition/removals.
    3. for 128b/130b encodings:
        1. Have the exercisers insert a SKPOS between every 371 blocks.
        2. Confirm that the retimer is adding 4 SKP symbols to at least 1 SKPOS per 38 * 10^4 blocks in the upstream direction.
        3. Confirm that the retimer is removing 4 SKP symbols to at least 1 SKPOS per 38 * 10^4 blocks in the downstream direction.
        4. Have the exerciser insert a SKPOS between every 374 blocks and confirm the above SKPOS addition/removals.

4.3 Latency Test

1. Place the DUT on a link between 2 exercisers.
2. For every data rate supported by the DUT:
    1. Get the retimer into a state where it is forwarding data without SRIS in both directions using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. Measure the time between when the upstream exerciser begins sending a packet to the retimer and when the downstream exerciser begins receiving the same packet from the retimer.
    3. Measure the time between when the downstream exerciser begins sending a packet to the retimer and when the upstream exerciser begins receiving the same packet from the retimer.
    4. Confirm that the measured times above do not exceed the values in Table 4-22 for the current data rate.
3. If SRIS is supported, for every data rate supported by the DUT:

1. For every max_payload_size listed in the PCIe specification:
    1. Get the retimer into a state where it is forwarding data with SRIS in both directions using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. measure the following times for all packets sent within a 100 µS window:
        1. from when the upstream exerciser begins sending a packet to the retimer to when the downstream exerciser begins receiving the same packet from the retimer.
        2. from when the downstream exerciser begins sending a packet to the retimer to when the upstream exerciser begins receiving the same packet from the retimer.
    3. Confirm that all the measured times above do not exceed the values in Table 4-23 for the current data rate.

4.4 Retimer Present and Parity Test

1. Place the DUT on a link between 2 exercisers.
2. For all data rates supported by the retimer:
    1. Get the retimer into a state where it is forwarding training sets at in both directions using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
    2. Send 4 consecutive identical TS1s with the First Retimer Present field clear.
    3. Confirm that the TS1s are forwarded by the retimer with the First Retimer Present field is set and the Second Retimer Present field clear.
    4. If operating at or above the 16GT/s data rate:
        1. Get the retimer into the lane margining state using the process described in Section 3.7 Lane Margining Macro .
        2. Send Control SKPOSes with Receiver number set to 000b.
        3. Send Control SKPOSes with Receiver number set to 001b.
        4. Confirm that the First Retimer Parity bit in the Control SKPOSes was different in the above 2 cases.
    5. Send 4 consecutive identical TS1s with the First Retimer Present field set.
    6. Confirm that the TS1s are forwarded by the retimer with the First Retimer Present field is set and the Second Retimer Present field set.
    7. If operating at or above the 16GT/s data rate:
        1. Get the retimer into the lane margining state using the process described in Section 3.7 Lane Margining Macro .
        2. Send Control SKPOSes with Receiver number set to 000b.
        3. Send Control SKPOSes with Receiver number set to 001b.
        4. Confirm that the Second Retimer Parity bit in the Control SKPOSes was different in the above 2 cases.

4.5 Forwarding Tests

4.5.1 Forwarding Packet and Symbol Non-error Test

1. Place the DUT on a link between 2 exercisers.
2. For all data rates supported by the DUT:
    1. Get the retimer into a state where it is forwarding data without SRIS in both directions using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. Inject from Upstream and Downstream exercisers sequences of TLPs and DLLPs.
    3. Confirm that the DUT forwards all the symbols unmodified except:
        - The TS1/TS2 fields listed in Section 4.3.6.7 of the PCIe 4.0 Base Specification.
        - The length of SKP OSs.
        - The Control SKP Orderded Set fields listed in Section 4.3.6.7 of the PCIe 4.0 Base Specification.
        - Symbols with a 8b/10b decode error or disparity error (see Section 4.3.6.9 of the PCIe 4.0 Base Specification).
    4. Confirm that all injected data received unchanged by the opposite side exerciser. The only permitted change in data is 8b/10b test case when symbol or disparity error happened on one of retimer's pseudoports.

4.5.2 Forwarding Symbol and Block Alignment Test

1. Place the DUT on a link between 2 exercisers.
2. For all 128b/130b data rates supported by the DUT:
    1. Get the retimer into a state where it is forwarding data without SRIS in both directions using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. Inject from Upstream and Downstream exercisers sequences of TLPs and DLLPs.
    3. Insert symbol errors and wrong block alignment header on part of packets stream.
    4. Confirm that all injected data received unchanged by the opposite side exerciser except:
        1. The length of SKP OSs.

4.5.3 Disable Scrambler Test

This test determines if a retimer forwards data unmodified regardless of whether Disable Scrambling is enabled or not.

1. For all 8b/10b data rates supported by the DUT:
    1. Get the retimer into a state where it is forwarding non-training sets using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. Inject the sequence of TLPs/DLLPs from the Upstream and Downstream exercisers.
    3. Confirm that the DUT forwards all the symbols unmodified except:
        - The TS1/TS2 fields listed in Section 4.3.6.7 of the PCIe 4.0 Base Specification.
        - The length of SKP OSs.
        - The Control SKP Orderded Set fields listed in Section 4.3.6.7 of the PCIe 4.0 Base Specification.
        - Symbols with a 8b/10b decode error or disparity error (see Section 4.3.6.9 of the PCIe 4.0 Base Specification).

2. Follow the procedure described in Section 3.1 Retimer Reset Macro to reset the retimer.
3. Disable the scrambler in both directions using the process described in Section 4.2.6.3.5 and repeat steps 1 and 2 above.

4.5.4 Inferred Electrical Idle Test

This test determines if a retimer follows the inferred electrical idle rules in section 4.3.6.5.

1. For every speed supported by the retimer:
    1. Enter electrical idle using the process described in Section 3.5 Electrical Idle Entry Macro .
    2. Send a single EIEOS on all lanes then wait.
    3. Confirm that Electrical idle is entered after the interval listed in Table 4-21 of the PCIe 4.0 Base Specification
    4. Exit electrical idle using the process described in Section 3.6 Electrical Idle Exit Macro .
    5. Get the retimer into a state where it is forwarding non-training sets using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro then wait.
    6. Confirm that Electrical idle is entered after the interval listed in Table 4-21 of the PCIe 4.0 Base Specification.
    7. Get the retimer into a state where it is forwarding training sets using the process described in Section 3.2 Retimer Training Set Forwarding Macro then wait.
    8. Confirm that Electrical idle is entered after the interval listed in Table 4-21 of the PCIe 4.0 Base Specification.
2. At the 2.5GT/s data rate:
    1. Enter Forwarding Loopback mode and wait.
    2. Confirm that Electrical idle is entered after the interval listed in Table 4-21 of the PCIe 4.0 Base Specification.
    3. If supported by the retimer, Enter Slave Loopback mode and wait.
    4. Confirm that Electrical idle is entered after the interval listed in Table 4-21 of the PCIe 4.0 Base Specification.

4.5.5 Dynamic Port Orientation Test

This test determines if a retimer can determine Upstream/Downstream port orientation dynamically

1. Place the DUT on a link between 2 exercisers.
2. Get the retimer into a state where it is forwarding training sets at in both directions using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
3. From one exerciser, send two consecutive TS1 Ordered Sets on all lanes with unique non-PAD Lane Numbers.
4. Confirm that the Pseudoport facing the exerciser which did not send the TS1s is identified as the 'Downstream Port' by:
    1. sending two consecutive TS1s with the Disable Link set to 1b on any lane of the Downstream port.
    2. Confirming that the retimer does not place either transmitter in electrical idle.

5. Confirm that the Pseudoport facing the exerciser which sent the TS1s is identified as the 'Upstream Port' by:
    1. sending two consecutive TS1s with the Disable Link set to 1b on any lane of the Upstream port.
    2. Confirming that the retimer places both transmitters in electrical idle.
6. Reset the retimer and Repeat the process above, but send the TS1s with unique Lane numbers from other exerciser to confirm that the retimer works in both orientations.

4.5.6 Link Width Test

This test determines if a retimer can support all spec-defined link widths from 1 to the maximum width supported by the retimer

1. Place the DUT on a link between 2 exercisers.
2. Begin forwarding Training Sets on all lanes in the link using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
3. After Configuration has completed, confirm that the retimer is forwarding on the appropriate number of lanes.
4. Reset the retimer and Repeat the above process for all link widths, from the next largest width supported by the retimer down to a x1 width.

4.5.7 Lane Reversal Test

This test determines if a retimer is interoperable with ports that support Lane Reversal

1. Place the DUT on a link between 2 exercisers.
2. Begin forwarding Training Sets on all lanes with Lane Numbers in Non-reversed order using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
3. Begin sending scrambled data using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
4. Confirm that the retimer Captured the correct Lane numbers by checking that each lane begins sending data with the proper seed value.
5. Repeat the above process, but send the Training Sets with reversed Lane Numbers.

4.5.8 Scrambling Modification Test

This test determines if a retimer forwards data unmodified regardless of whether Disable Scrambling is enabled or not

1. For all 8/10b data rates supported by the DUT:
    1. Get the retimer into a state where it is forwarding data in both directions using the process described in Section 3.3 Retimer Non-Training Set Forwarding Macro .
    2. Inject from Upstream and Downstream exercisers sequences of TLPs and DLLPs.
    3. Confirm that the DUT forwards all the symbols unmodified except:

- The TS1/TS2 fields listed in Section 4.3.6.7 of the PCIe 4.0 Base Specification.
- The length of SKP OSs.
- The Control SKP Orderded Set fields listed in Section 4.3.6.7 of the PCIe 4.0 Base Specification.
- Symbols with a 8b/10b decode error or disparity error (see Section 4.3.6.9 of the PCIe 4.0 Base Specification).

2. Confirm that all injected data received unchanged by the opposite side exerciser. The only permitted change in data is 8b/10b test case when symbol or disparity error happened on one of retimer's pseudoports
3. Follow the procedure described in Section 3.1 Retimer Reset Macro to reset the retimer.
4. Disable scrambler in both directions as described in Section 4.2.6.3.5 of the PCIe 4.0 Base Specification.
5. Repeat steps 1 and 2 for unscrambled TLPs and DLLPs

4.5.9 Lane Polarity Detection Test

This test determines if a retimer determines lane polarity every time Symbol Lock is achieved at 2.5GT/s

1. Place the DUT on a link between 2 exercisers.
2. Begin transmitting non-inverted Training Sets from both exercisers using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
3. Confirm that all Training Sets forwarded by the retimer were not inverted.
4. Repeat steps 2 and 3, but invert the Training Sets being sent upstream.
5. Repeat steps 2 and 3, but invert the Training Sets being sent downstream.
6. Repeat steps 2 and 3, but invert the Training Sets being sent by both exercisers(ie: the retimer should be uninverting any inverted data sent by the exerciser).

4.5.10 Polarity Inversion Test

This test determines if a retimer correctly inverts the polarity transmitted data (when necessary).

1. Place the DUT on a link between 2 exercisers.
2. Enter Electrical Idle using the process described in Section 3.5 Electrical Idle Entry Macro .
3. Exit Electrical Idle and begin forwarding non-inverted training sets using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
4. Confirm that the retimer forwards training sets without inverting the data.
5. Enter Electrical Idle using the process described in Section 3.5 Electrical Idle Entry Macro .
6. Exit Electrical Idle and begin forwarding inverted training sets using the process described in Section 3.2 Retimer Training Set Forwarding Macro .
7. Confirm that the retimer forwards training sets and properly inverts the transmitted data.
8. Confirm that the output of the pesudoports is identical in both the inverted and non-inverted case. (ie: the retimer should be uninverting any inverted data sent by the exerciser).

4.5.11 Control SKP OS Modification Test

This test determines if a retimer modifies the required portions of a Control SKP OS (AKA the last 3 bytes) while leaving the remainder unmodified.

1. At the 16GT/s data rate:
    1. Get the retimer into the lane margining state using the process described in Section 3.7 Lane Margining Macro .
    2. Send Control SKPOSes to the retimer with the commands listed in Table 4-1 Retimer Margin Commands sequentially.
    3. Confirm that for each request the retimer sends the appropriate response SKPOS listed in Table 4-2 Retimer Margin Expected Responses .

Table 4-1 Retimer Margin Commands

Test		Command	
Command Name	Test If	Type [2:0]	Payload [7:0]
Access Retimer register	Always Test	001b	00h
Report Margin Control Capabilities	Always Test	001b	88h
Report $M_{NumVoltageSteps}$	If $M_{VoltageSupported}$ = 1b	001b	89h
Report $M_{NumTimingSteps}$	Always Test	001b	8Ah
Report $M_{MaxTimingOffset}$	Always Test	001b	8Bh
Report $M_{MaxVoltageOffset}$	If $M_{VoltageSupported}$ = 1b	001b	8Ch
Report $M_{SamplingRateVoltage}$	If $M_{SampleReportingMethod}$ = 1b	001b	8Ch
Report $M_{SamplingRateTiming}$	If $M_{SampleReportingMethod}$ = 1b	001b	8Eh
Report $M_{SampleCount}$	Always Test	001b	8Fh
Report $M_{MaxLanes}$	Always Test	001b	90h
Set Error Count Limit	Always Test	010b	[7:6] 11b [5:0] 0-31
Go to Normal Settings	Always Test	010b	0Fh
Clear Error Log	Always Test	010b	55h

Test		Command	
Command Name	Test If	Type [2:0]	Payload [7:0]
Step Margin timing offset to right/left of default	Always Test	011b	If $M_{IndLeftRightTiming}$ is set: 7 Reserved 6 if Set left, if clear right [5:0] steps left or right If $M_{IndLeftRightTiming}$ is clear: [7:6] Reserved [5:0] steps beyond normal setting
Step Margin voltage offset to up/down of default	Always Test	100b	If $M_{IndUpDownVoltage}$ is set: 7 if Set Down, if Clear Up [6:0] steps down or up If $M_{IndUpDownVoltage}$ is clear: [7:6] Reserved [6:0] steps beyond normal setting

Table 4-2 Retimer Margin Expected Responses

Test	Response	
Command Name	Type [2:0]	Payload [7:0]
Access Retimer register	001b	0-255
Report Margin Control Capabilities	001b	0-31
Report $M_{NumVoltageSteps}$	001b	32-127
Report $M_{NumTimingSteps}$	001b	6-63
Report $M_{MaxTimingOffset}$	001b	0,20-50
Report $M_{MaxVoltageOffset}$	001b	0, 5-50
Report $M_{SamplingRateVoltage}$	001b	0-63
Report $M_{SamplingRateTiming}$	001b	0-63
Report $M_{SampleCount}$	001b	0-127
Report $M_{MaxLanes}$	001b	0-31
Set Error Count Limit	010b	Same as Request
Go to Normal Settings	010b	0Fh
Clear Error Log	010b	55h

Test	Response	
Command Name	Type [2:0]	Payload [7:0]
Step Margin timing offset to right/left of default	011b	0-255
Step Margin voltage offset to up/down of default	100b	0-255

4.6 Loopback Tests

This section contains tests which determines if a retimer meets loopback requirements.

4.6.1 Forwarding Loopback Test

Retimers must support Forwarding between 2 Ports that are in Loopback. Retimers must not cause a known-good device to fail the tests listed in section 3.8 of the PCI Express Architecture Link Layer and Transaction Layer Test Specification, Revision 4.0. Note that in these tests some timing requirements are increased when retimers are present

1. Place the DUT on a link between an exerciser and a "known-good" device that passes the tests listed in section 3.8 of the PCI Express Architecture Link Layer and Transaction Layer Test Specification, Revision 4.0. It is permitted for the "known-good" device to be another exerciser.
2. Confirm that the "known-good" device passes the tests listed in section 3.8 of the PCI Express Architecture Link Layer and Transaction Layer Test Specification, Revision 4.0 when the retimer is present.

4.6.2 Slave Loopback Test (Optional)

Pseudoports on retimer which supports Slave Loopback must pass the tests listed in section 3.8 of the PCI Express Architecture Link Layer and Transaction Layer Test Specification, Revision 4.0, when the "Pseudo Port Slave Loopback" configuration parameter is set to Slave Loopback mode. Since retimers are required to determine port orientation dynamically, pseudoports are required to pass both the Upstream and Downstream port tests.

4.7 Link Layer Tests

In addition to the tests listed in this document, retimers are also required to pass the following tests from the PCI Express Architecture Link Layer and Transaction Layer Test Specification, Revision 4.0:

Table 4-3 Required Tests from the Link Layer and Transaction Layer Test Specification

Name	Reference Number	Subsection(s)
Reserved Bits in Training Sequences: Endpoint Device	55-10	3.5.1

Name	Reference Number	Subsection(s)
Reserved Bits in Training Sequences: Root Port	55-10	3.5.2
De-emphasis Request During Speed Change	56-10	3.6
Link Equalization: Adjusting Initial Preset for 8.0 GT/s	57-10	3.7.1
Link Equalization: Adjusting Initial Preset for 16.0 GT/s	57-11	3.7.2
Link Equalization: Adjusting Presets for 8.0 GT/s	58-10	3.7.3
Link Equalization: Adjusting Presets for 16.0 GT/s	58-11	3.7.4
Link Equalization: Adjusting Coefficients for 8.0 GT/s	59-10	3.7.5
Link Equalization: Adjusting Coefficients for 16.0 GT/s	59-11	3.7.6
Link Equalization: Equalization Redo for 16.0 GT/s	5x-11	3.7.7

5. Inteoperability Tests

Retimers are required to show that a downstream device is interoperable with a host when connected through the retimer by meeting the requirements listed in the PCI Express Interoperability User Guide, Version 1.0.